AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A Test Structure for verifying an isolation trench etching in an SOI wafer, wherein the test structure comprises, after etching of isolation trenches, a row of connected islands, each of which is surrounded by a trench, said trenches having an (step-wise) increasing width from island to island (A, B; B,C), including a trench width of an isolation trench of an active circuit;

- wherein a section (part) of the surrounding trench (a, b) of each island (A, B) forms a common part with the trench of the adjacent island;

- wherein the respective section - except for the island having the broadest (e) or the narrowest (a) isolation trench - has the width of the adjacent trench having the next larger or the next smaller measure of width in the row.

2. (Original) A Method of verifying insulation trench etchings or isolation trench etchings in SOI substrates, comprising

- forming a test structure comprising a row of successive islands during an etch process or preparing the test structure for an etch process and measuring an electric pass several times during or after said trench etching;

- wherein a plurality of measurements of the electric pass are performed;

- wherein one of the measurements is performed between two adjacent islands (A, B), a further measurement is performed between other adjacent islands (B, C);
- using measurement values of said plurality of measurements for assessing a sufficient or appropriate depth of etched insulation trenches or isolation trenches located in particular outside said test structure above said substrate in an area of an active circuit.

3. (Original) A Method for verifying trench etchings (isolation trench, insulation trench) in an SOI substrate, comprising

- preparing a test structure (A, B, D, E) above the substrate and forming the test structure during a trench etching and measuring after or during said trench etching an electric pass particularly successively between an island (A, B) and the substrate region (S) at least partially surrounding said island and
- using the magnitude or the amount of the measurement results for assessing or detecting a sufficient or appropriate depth of etched trenches located in particular outside said test structure but being formed during said trench etching.

4. (Currently Amended) The method of ~~claims 2 or 3~~ claim 2, wherein said test structure ~~is the test structure of claim 1~~ comprises, after etching of isolation trenches, a row of connected islands, each of which is surrounded by a trench, said trenches having an (step-wise) increasing width from island to island (A, B; B,C), including a trench width of an isolation trench of an active circuit;

- wherein a section (part) of the surrounding trench (a, b) of each island (A, B) forms a common part with the trench of the adjacent island;

- wherein the respective section - except for the island having the broadest (e) or the narrowest (a) isolation trench - has the width of the adjacent trench having the next larger or the next smaller measure of width in the row.

5. (Currently Amended) The method of ~~claims 2 or 3~~ claim 2, wherein said electric pass is a resistance or a conductance.

6. (Currently Amended) The method of ~~claims 2 or 3~~ claim 2, wherein said pass is a current at a constant voltage 20 or a voltage measurement at a constant current.

7. (Currently Amended) The method of ~~claims 2 or 3~~ claim 2, wherein the measurements are performed during the etch process, and wherein the etch process is interrupted to perform in particular the successive measurement on the islands.

8. (Original) The method of claim 7, wherein the etching (etch process) is continued when the trench having a width (d) corresponding to the present circuit is

not completely etched through to the insulating layer (1).

9. (Currently Amended) The method of ~~claims 7 or 8~~ claim 7, wherein the etching is stopped, when the trench having a width (d) corresponding to the active circuit is etched through to the insulating layer (1).

10. (Original) A Method for verifying insulation trench etchings in SOI wafers, in which dedicated devices or complete circuit modules are laterally dielectrically isolated in the form of islands from the surrounding region by enclosing insulation trenches (8);

by a test structure prepared on an individual wafer, for performing a verification of the electric resistances or resistance during a process step "insulation trench etch process"

between specific regions (A,B; B,C) of the test structure and/or

between specific regions of the test structure and the surrounding crystal region (S)

the method further comprising

- preparing the test structure on the wafer, said test structure having a row of connected islands after the trench etch process of the process step "insulation trench etch process", each island being surrounded by a trench having a different width between respective two of said islands;
- wherein the width of the insulation trench provided in the active circuit is positioned approximately in a central location within said row of islands,

and a portion of the length of the surrounding trench of each island, except for the outer most island, defines a shared piece of the island of a respective adjacent island such that said portion of the length particularly corresponds to the width of the adjacent trench having the next larger or the next smaller measure of width in the row;

- after the etch process of the "insulation trench etch process", assessing a proper process result by repeatedly verifying the electric pass between respective two adjacent islands or between a respective island and the surrounding (S) of said respective island outside of said test structure;
- using an amount of one or more detected measurement values of the measurement as a measure or a test for the target depth, in particular for the predefined depth, of etched insulation trenches or isolation trenches (8).

11. (Original) The method of claim 10, wherein the width of each trench surrounding a respective island in the row of islands receives an increasing width that increases in a step-wise manner from island to island.

12. (Original) The method of claim 10, wherein a width of the insulation trench (8) occurring in the active circuit is predefined as a "relevant width of insulation trenches".

13. (Currently Amended) The method of ~~any of claims 2, 3 or 10~~ claim 2, wherein, during a successive measurement of passes, it is started with an island having a surrounding trench width (d) that substantially corresponds to one or more relevant insulation trenches (8) of the circuit.

14. (Currently Amended) The method of ~~claims 2 or 12~~ claim 2, wherein the step of verifying is completed after two measurements, when an abrupt change of the pass value for the total insulation (etching through the insulating layer) is obtained for the relevant pair of islands of the test structure, and when testing the adjacent pair of islands having the smaller trench width does not exhibit said abruptly changed measurement value.

15. (Currently Amended) The method or the test device of ~~any of the preceding claims~~ claim 2, wherein at least three, preferably five or more island regions (A to E) are connected to each other.

16. (Currently Amended) The method of ~~claims 2 or 3 or 10~~ claim 2, wherein not more than n-1 measurements are performed for the n islands, n being the number of islands in said row.

17. (Currently Amended) The method of ~~claims 2 or 3 or 10~~ claim 2, wherein the maximum number of measurements between islands and the surrounding (S) corresponds to the number of islands in the row of islands.

18. (Currently Amended) The method of ~~claims 2 or 3~~ claim 2, wherein after the etch process the measurement results are evaluated, and wherein particularly further etch processes of following wafers are adapted with respect to their target etch time to the result of the preceding measurements.

19. (Original) The method of claim 10, wherein the step of preparing is performed by a predetermined mask.